

WHAT IS CLAIMED IS:

- 1 1. A high frequency bus system comprising:
2 a first bus segment having at least one device
3 connection between a first and a second end, the first bus
4 segment comprising at least two transmission lines for
5 propagating high frequency signals, the at least one device
6 coupled to the at least two transmission lines;
7 a second bus segment being free of device
8 connections and having a first and a second end, the second
9 bus segment comprising at least two transmission lines for
10 propagating high frequency signals;
11 means for coupling the second end of the second bus
12 segment to the first end of the first bus segment in series to
13 form a chain of segments; and
14 wherein the at least two signals introduced at the
15 first end of the second bus segment at the substantially the
16 same time, arrive at each device connected to the first bus
17 segment at substantially the same time.
- 1 2. The bus system of claim 1, wherein signals
2 originating from the at least one device on the first bus
3 segment substantially at the same time, arrive at the first
4 end of the second bus segment at substantially the same time.
- 1 3. The bus system of claim 1, further comprising a
2 module on which the first bus segment is routed, wherein the
3 at least one device is mounted on the module and further
4 comprising a motherboard on which the second bus segment is
5 routed.
- 1 4. The bus system of claim 3, wherein the means
2 for coupling comprises through-holes on the motherboard and
3 pins on the module, the pins being coupled to the transmission
4 lines at the first end of the first bus segment, the
5 through-holes being coupled to the transmission lines at the
6 second end of the second bus segment and receiving the solder
7 pins of the module to couple the first and second bus segments.

1 5. The bus system of claim 3, wherein the means
2 for coupling comprises a socket on the motherboard and edge
3 fingers on the module, the edge fingers being coupled to the
4 transmission lines at the first end of the first bus segment,
5 the socket being coupled to the transmission lines at the
6 second end of the second bus segment and receiving the edge
7 fingers of the module to couple the first and second bus
8 segments.

1 6. The bus system of claim 5, further comprising a
2 capacitive structure on the motherboard located between the
3 transmission lines of the second bus segment and the socket on
4 the mother board, wherein the transmission lines of the first
5 and second bus segments have substantially the same impedance,
6 wherein the socket on the motherboard has a certain inherent
7 inductance and capacitance, wherein the edge finger on the
8 module comprises a capacitive structure on the module, and
9 wherein the combination of the socket capacitance, the edge
10 finger capacitance, the motherboard capacitive structure and
11 the socket inductance has an impedance matching the impedance
12 of the first and second bus segments.

1 7. The bus system of claim 1, wherein the
2 transmission lines of the first bus segment are routed with a
3 right angle turn between the coupling means and the at least
4 one device, wherein the transmission lines on a first side of
5 the right angle turn coupled to the at least one device have a
6 stripline construction, wherein the transmission lines on a
7 second side of the right angle turn have a microstrip
8 construction, and wherein the transmission lines on the two
9 sides of the right angle turn are coupled by means of
10 conductive feed-through holes.

1 8. The bus system of claim 7, wherein the
2 stripline construction has the same impedance as the
3 microstrip construction.

1 9. The bus system of claim 8, wherein the
2 stripline construction comprises two conductive tracks running
3 in parallel and connected to the same microstrip at the
4 location of the feed-through hole.

1 10. The bus system of claim 7, wherein the at least
2 one device is coupled to the first side of the right angle
3 turn by transmission lines having a stripline construction,
4 the striplines having an unloaded impedance higher than the
5 impedance of the lines on the first side of the right angle
6 turn and having a loaded impedance equal to the impedance of
7 the lines on the first side of the right angle turn.

1 11. The bus system of claim 7, wherein the at least
2 one device is coupled to the first side of the right angle
3 turn by transmission lines having a microstrip construction,
4 the microstrips having an unloaded impedance higher than the
5 impedance of the lines on the first side of the right angle turn
6 and having a loaded impedance equal to the impedance of the
7 lines on the first side of the right angle turn.

1 12. The bus system of claim 7, further comprising
2 lengths of delay matching transmission lines inserted between
3 the second side of the right angle turn and the feed-through
4 holes coupling the two sides of the right angle turn, the
5 length of the delay matching lines being such as to assure
6 that signals arriving substantially at the same time at the
7 coupling means arrive substantially at the same time at the at
8 least one device.

1 13. A high frequency bus system comprising:
2 a motherboard having a first bus segment;
3 a bus termination on said motherboard which is
4 isolated from said first bus segment on said mother
5 board;

6 at least one memory module having a second bus
7 segment connected to said first bus segment at a first
8 end, and connected at a second end to said bus
9 termination on said motherboard.

WPA1